

# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2002-184126

(43)Date of publication of application : 28.06.2002

(51)Int.Cl.

G11B 20/14  
G11B 20/10  
H03L 7/10

(21)Application number : 2000-379288

(71)Applicant : MATSUSHITA ELECTRIC IND CO  
LTD

(22)Date of filing : 13.12.2000

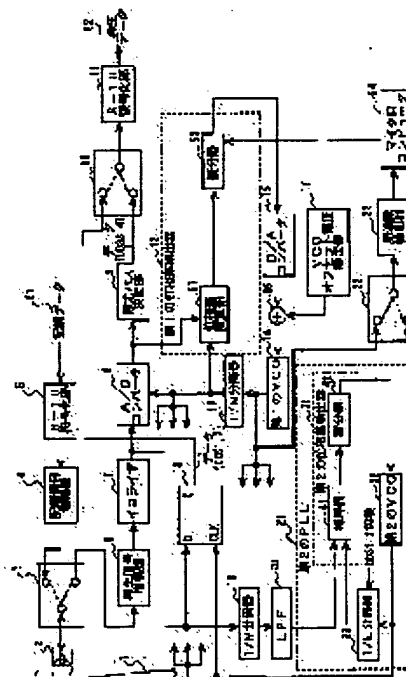
(72)Inventor : AOKI TSUKASA

## (54) CLOCK SIGNAL GENERATING DEVICE FOR REPRODUCED SIGNAL

### (57)Abstract:

**PROBLEM TO BE SOLVED:** To provide the clock signal generating device of a reproduced signal having a digital PLL(phase-locked loop) which has a capture range equal to that of the conventional analog PLL and in which a phase is locked even at the search time of, for example, a helical scanning type magnetic reproducing device.

**SOLUTION:** This clock signal generating device of the reproduced signal has a digital PLL and an analog PLL and controls the digital PLL so that the frequency of the digital PLL and the frequency of the analog PLL become the same by detecting frequencies of respective output signals of the analog PLL and the digital PLL.



## LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision  
of rejection]

[Date of requesting appeal against examiner's  
decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office